Changes in the Editorial Board

(See next page)

AFTER nine years (the maximum three consecutive terms) on the Editorial Board of the IEEE TRANSACTIONS ON ELECTRON DEVICES (TED), Prof. Richard Carter, Lancaster University, U.K. (Vacuum Electron Devices), Dr. Youichi Momiyama, Socionext, Japan (MOS Devices and Technology), Prof. Guofu Niu, Auburn University, USA (Bipolar Devices), and Prof. Rama Venkatasubramanian, Johns Hopkins Applied Physics Lab, USA (Thermal Management) have stepped down from their Editor positions in the respective fields.

After six years on the TED Editorial Board, Prof. Muhannad Bakir, Georgia Institute of Technology, USA (MOS Devices and Technology) and Dr. Ravi Todi, Qualcomm Technologies, USA (MOS Devices and Technology) have stepped down from their Editor positions in the respective fields.

After five years on the TED Editorial Board, Prof. Yong-Young Noh, Pohang University of Science and Technology, Korea, has stepped down from his Editor position in the field of Molecular and Organic Devices.

I would like to express my sincere gratitude—and the gratitude of the Electron Device Society (EDS) community at large—to Richard, Youichi, Guofu, Rama, Muhannad, and Ravi for their commitment, dedication, and hard work during their term of service. Our very best wishes to them in their future endeavors.

At the same time, I am more than glad to announce that ten new Editors have joined the TED Editorial Board during the first half of the year 2020. They are not only meant to replace some of the retiring ones but also to bring within TED's new expertise and enthusiasm to the job and to further strengthen their areas. All of them are recognized experts in their own field. They are Dr. Nuo Xu from TSMC, USA (Device and Process Modeling), Prof. Rihito Kuroda from Tohoku University, Japan (Image Sensors), Dr. Syed M. Alam from Everspin, USA (Memory Devices and Technology), Dr. Pritish Narayanan from IBM, USA (Memory Devices and Technology), Dr. Paragkumar A. Thadesar from Qualcomm Technologies, USA (MOS Devices and Technology), Prof. Jamie Phillips from the University of Michigan, USA (Optoelectronic Devices), Prof. John F. Conley from Oregon State University, USA (Thin-Film Transistors), Prof. Jin-Seong Park from Hanyang University, Korea (Thin-Film Transistors), Prof. Samuel Graham from Georgia Institute of Technology, USA (Thermal Management), and Dr. Rosa Letizia from Lancaster University, U.K. (Vacuum Electron Devices).

A warm welcome to the newly appointed Editors!

GIOVANNI GHIONE, *Editor-in-Chief*
Politecnico di Torino
Turin, Italy

Nuo Xu received the B.Sc. degree in microelectronics from Peking University, Beijing, China, in 2008, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, Berkeley, CA, USA, in 2010 and 2012, respectively. His Ph.D. thesis was about Strain-Si Thin-body Transistor Technologies.

He has been with Synopsys, Mountain View, CA, in 2010 and imec, Leuven, Belgium, in 2011 for temporary positions. He became a Post-Doctoral Scholar and Lecturer in EE of UC Berkeley in 2012, researching on 3-D integration of emerging logic and memory devices and design-technology co-optimization (DTCO). He joined Samsung America Headquarters, Device Solutions (AHQ-DS), San Jose, CA, in 2014, as a Senior Staff Research Scientist, working on emerging nonvolatile memories (NVM), DTCO, and EDA/CAD algorithm development. He joined TSMC, San Jose, North America in 2019, as an R&D Manager, focusing on developing leading-edge NVM technologies, compact modeling, and EDA/CAD methodologies. He has published over 100 technical articles on peer-reviewed journals and conferences [including 12 IEEE International Electron Devices Meeting (IEDM)/IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) articles as the first author] and applied/been granted for over ten U.S. patents.

Dr. Xu is a member of the IEEE Electron Devices Society (EDS) Technical Committee on Technology CAD and served as the Sub-Committee Chair (2020) and a member (2018–2019) for IEEE IEDM Modeling and Simulation Sessions. He was a recipient of the IEEE EDS Student Fellowship (2010), the TSMC Academia Award for Outstanding Student (2012), and the Samsung AHQ-DS President Award (2019).

Digital Object Identifier 10.1109/TED.2020.3032222

Paragkumar A. Thadesar received the B.E. degree in electronics and communication engineering with a gold medal from V.V.P. Engineering College, Rajkot, Gujarat, in 2009, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011 and 2015, respectively. His Ph.D. research was focused on electrical design, fabrication and high-frequency characterization of through-silicon vias (TSVs) and radio-frequency (RF) platforms for 2.5-D integration using silicon interposers.

He is an RF Front-End IC/Module Design Engineer at Qualcomm, San Diego, CA, USA, since 2015. His research interests include interconnects, advanced packaging, and radio-frequency integrated circuits.

Dr. Thadesar received the IBM Ph.D. Fellowship Award from 2014 to 2015, the Outstanding Interactive Presentation Paper Award at the IEEE Electronic Components and Technology Conference in 2013, a Best-in-Session Award at Semiconductor Research Corporation TECHCON, Austin, TX, USA, in 2013, the Third Place Microelectronics Foundation Prize at IMAPS Device Packaging, Fountain Hills, AZ, USA, in 2013, and the Best Student Paper Awards at the Global Interposer Technology Workshop in 2011 and 2012. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY and the Chapter Chair for the IEEE San Diego Electronics Packaging Society (EPS) chapter.

Jamie Phillips received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1994, 1996, and 1998, respectively.

He is currently a Professor and Chair of the ECE Department with the University of Delaware, Newark, DE, USA. He was a Post-Doctoral Researcher with Sandia National Labs, Albuquerque, NM, USA, from 1998 to 1999 and Research Scientist with the Rockwell Science Center, Thousand Oaks, CA, USA, from 1999 to 2001 before returning to the University of Michigan as a Faculty Member in 2002. At the University of Michigan, he was an Arthur F. Thurnau Professor with the EECS Department prior to joining the University of Delaware in 2020. His expertise is in the growth, characterization, and device applications of compound semiconductor and oxide-based materials for optoelectronics and electronics in which he has published more than 130 peer-reviewed journal articles.

Dr. Phillips received the NSF CAREER Award, DARPA MTO Young Faculty Award, the IEEE Paul Rappaport Best Paper Award, and the IEEE Theodore E. Batchman Best Paper Award.

John F. Conley, Jr. (Fellow, IEEE) received the B.S. degree in electrical engineering and the Ph.D. degree in engineering science and mechanics from The Pennsylvania State University, State College, PA, USA, in 1991 and 1995, respectively, where he won a Xerox Award for his Ph.D. dissertation.

Since 2007, he is a Professor of both electrical engineering and computer science and materials science with Oregon State University, Corvallis, OR, USA, where he is the Director of the Materials Synthesis and Characterization (MASC) facility. He has also engaged as a technical consultant and expert witness. Previously, he was a Senior Member of the technical staff at both Dynamics Research Corporation and the NASA Jet Propulsion Laboratory, the Leader of the Novel Materials and Devices Group at Sharp Laboratories of America, and an Adjunct Professor with Washington State University, Pullman, WA, USA. His current research interests include atomic layer deposition (ALD) development of novel materials for application in metal/insulator/metal devices (MIM & MIIM tunnel diodes), MIM high-κ capacitors, RRAM and amorphous oxide semiconductor thin-film transistors (TFTs), internal photoemission (IPE), nanomaterials, and sensors. He has authored or coauthored over 150 journal and/or conference papers; over 160 additional conference presentations (including two tutorial short courses and more than 20 invited talks at international conferences); more than 40 invited talks at universities, government labs, and companies; and 20 U.S. patents.

Dr. Conley has served on the technical and organizing committees of numerous IEEE (IRPS, IRW, SOI, IEDM, NSREC, Nano, MRQW), American Vacuum Society (AVS), and Material Research Society (MRS) meetings; as the Program Chair of the AVS International Conference on Atomic Layer Deposition (ALD) and IEEE IRW; and multiple times as a Guest Editor for IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY (T-DMR). He is a fellow of the AVS and the Oregon Nanoscience and Microtechnologies Institute (ONAMI).

Rihito Kuroda received the B.S. degree in electronic engineering and the M.S. and Ph.D. degrees in management science and technology from Tohoku University, Sendai, Japan, in 2005, 2007, and 2010, respectively.

He was a Research Fellow of the Japan Society for the Promotion of Science Research from 2007 to 2010. Since 2010, he is with the Graduate School of Engineering, Tohoku University, where he is currently an Associate Professor. He is engaged in studies on the process, device, design, and characterization of advanced CMOS image sensors.

Dr. Kuroda received the 2016 nac High Speed Imaging Award. He has been serving as a Committee Member of IEEE International Electron Devices Meeting (IEDM) since 2015, IEEE Sensors in 2014–2016, *Journal of Electronic Imaging* since 2015, and several other international conferences, and a board director of the International Image Sensor Society since 2017.

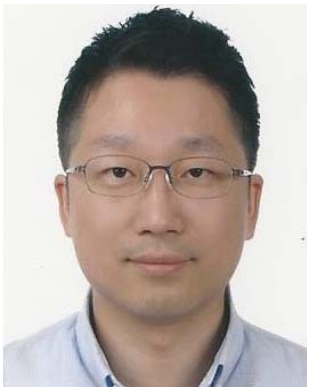
Syed M. Alam received the B.S. degree in electrical engineering from The University of Texas at Austin, Austin, TX, USA, in 1999, and the M.S. and Ph.D. degrees in electrical engineering and computer science from MIT, Cambridge, MA, USA, in 2001 and 2004, respectively.

He is the Director of Design Engineering at Everspin Technologies, Lexington, MA, leading the design functional areas and pathfinding for roadmap and technology advancement for STT-MRAM. He has worked on various aspects of memory device and design, including array circuits and architecture, and new product introduction supporting test, reliability, bitcell characterization, and high-speed interface characterization for STT-MRAM. He has mentored/co-advised five Ph.D. students for research on 3-D integration and logic-in-memory architecture. He has over 80 issued U.S. patents and over 65 journal/conference publications.

Pritish Narayanan received the B.E. (Hons.) and M.Sc. (Hons.) degrees in electrical engineering and chemistry, respectively, from the Birla Institute of Technology and Science (BITS), Pilani, India, both in 2005 and the Ph.D. degree in electrical and computer engineering from the University of Massachusetts Amherst, Amherst, MA, USA, in 2013.

He joined IBM Research–Almaden, San Jose, CA, USA, as a Research Staff Member in 2013 as part of the Storage Class Memory project, where he investigated device and circuit design challenges for access devices used in 3-D crosspoint memory. His current research interests are in the area of ultra-high-performance hardware systems for artificial intelligence. His work focuses on novel non-Von Neumann architectures based on emerging nonvolatile memory, and he is the Lead Circuit Architect for several deep learning test sites based on phase change memory (PCM) and mixed-signal hardware.

Dr. Narayanan has presented two keynotes (International Memory Workshop 2017, Cool Chips 2018) and a tutorial session (Device Research Conference 2017), in addition to several invited talks. He won Best Paper Awards at the IEEE Computer Society Symposium on VLSI 2008 and at Nanoarch 2013. He has also been a Guest Editor for the *Journal of Emerging Technologies in Computing*, the Program Chair at IEEE Nanoarch 2015, and the Special Session Chair for IEEE Nano 2016, and has served on the Technical Program Committees of several conferences.



Jin-Seong Park received the B.S. degree from the Department of Material Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, in 1997, and the M.S. and Ph.D. degrees in plasma-enhanced atomic layer deposition from KAIST, in 1999 and 2002, respectively.

From 2003 to 2005, he was a post-doctor in chemistry and chemical biology, Harvard University, Cambridge, MA, USA. Then, he started to work as a Senior Researcher to develop advanced thin film transistor such based on organic semiconductor and amorphous oxide semiconductor for (flexible) active matrix organic light emitting display (AMOLED) in Samsung SDI (2005–2009), and Samsung Mobile Display (2008–2009, before Samsung Display), respectively. From 2009 to 2013, he was an Assistant Professor with the Department of Materials Science and Engineering, Dankook University, Cheonan, Republic of Korea. Since March 1, 2013, he has been with the Division of Material Science and Engineering, Hanyang University, Seoul, Republic of Korea, where he was first an Associate Professor and is currently a Full-Tenured Professor. His main research interests include the development of the functional thin film (such as atomic layer deposition) and devices for flexible/transparent/wearable electronics. He is also interested in the development of high-mobility semiconductors and the atmosphere pressure process for next-generation electronics (Semiconductor and Display Industry).

Dr. Park is a member of the Korean Information Display Society, the Society of Information Display, the Material Research Society (MRS) of Korea, and so on. He has served on the Executive Committee of the Thin Film Division of the American Vacuum Society (AVS) as well as the International Atomic Layer Deposition Conference.

Samuel Graham, Jr. received the B.S. degree in mechanical engineering from Florida State University, Tallahassee, FL, USA, in 1993 and the Ph.D. degree in mechanical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 1999.

He is the Eugene C. Gwaltney, Jr. Professor in the Woodruff School of Mechanical at the Georgia Institute of Technology. He holds a joint appointment with the National Renewable Energy Laboratory, Golden, CO, USA. His current research centers on the development of electronics made from wide bandgap semiconductors (III–V, oxides) and organic electronics for a range of applications, including displays, RF communications, power switches, neuromorphic computing, and flexible electronics. His research in the area of wide bandgap semiconductors addresses the engineering of the thermal response of the devices in order to enhance heat dissipation and improve device reliability. Key aspects of this work include thermal metrology of devices, understanding electrothermal phenomena, measuring thermal properties, and developing the understanding to create interfaces within the devices to control thermal transport. For neuromorphic devices, he is creating physics-based models and experimental tools to design the electro-thermal-ionic transport response that controls the set/reset behavior. From 1999 to 2003, he was a Sr. Member of Technical Staff at Sandia National Laboratory, Livermore, CA, USA, where he worked on the development of optical coatings for EUV lithography systems. In 2003, he joined the Woodruff School of Mechanical Engineering at the Georgia Institute of Technology as an Assistant Professor. He was promoted to a Professor in 2013 and is now the Eugene C. Gwaltney, Jr. Professor and School Chair.

Dr. Graham was a member of the Defense Science Study Group (2014–2016) and is a member of the Review Board of the Engineering Science Research Foundation of Sandia National Laboratory and the Emerging Technologies Technical Advisory Group for the U.S. Department of Commerce.

Rosa Letizia (Senior Member, IEEE) received the Laurea degree in electronic engineering from the Polytechnic of Bari, Bari, Italy, and the Ph.D. degree in computational photonics from the University of Leeds, Leeds, U.K., in 2005 and 2009, respectively.

In 2011, she joined the Engineering Department, Lancaster University, Lancaster, U.K., and the Cockcroft Institute of Accelerator Science and Technology, Warrington, U.K., where she has been a Senior Lecturer since 2019. Her research focuses on the design, fabrication and test of electromagnetic structures for the design of millimeter-wave and THz vacuum electron devices and high-frequency particle acceleration. Her expertise includes the development of computational modeling of complex electromagnetic structures from the millimeter-wave to the optical frequency range of the spectrum. She has published in excess of 90 peer-reviewed international journal and conference papers.

Dr. Letizia was the recipient of the Senior Research Fellowship from The Leverhulme Trust and Royal Academy of Engineering in 2019. She has served as a member of the Technical Committee for the U.K., Europe, China Millimeter Waves and Terahertz Technology Workshop (UCMMT) from 2013 to 2015 and the International Vacuum Electronics Conference (IVEC) in 2017. She serves as an Associate Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES.